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# HEMT Technology and Applications in Astrophysics

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**Special Thanks to:**

**Lorene Samoska**

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**Neal Erickson**

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**Piotr Starski**

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## Low Noise Amplifiers



Low Noise Amplifiers (LNAs) can be used as receiver front ends for systems at operating frequencies as high as 240 GHz. Cryogenic LNAs are competitive with other low noise technologies at frequencies as high as 100 GHz. They play a critical role in IF amplification for SIS heterodyne receivers.

### Figures of merit:

$$\Delta T = kT_{\text{sys}} / \sqrt{\beta\tau}$$

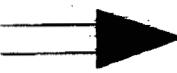
$\Delta T$  is measurement uncertainty (noise)

$T_{\text{sys}}$  is the receiver noise temperature

$\beta$  is the receiver bandwidth

$\tau$  is the integration (observation) time

$k$  is a constant (for gain stability or chop)



Decrease

$T_{\text{sys}}, k$

Increase

$\tau, \beta$  (for continuum obs.)



## InP HEMT Technology



InP High Electron Mobility Transistors offer the lowest noise, highest operating frequency and lowest power consumption of any millimeter wave transistor:

These advances have been spearheaded by:

- Processing improvements epixatial materials
- Short gate lengths using e-beam lithography
- Monolithic millimeter-wave integrated circuit (MMIC) processing advances:

- repeatability
- low parasitics

MMIC process iteration is slow and expensive



## Cryogenic HEMT Optimization Program (CHOP)



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TRW  
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NASA/GSFC  
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UMass  
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MPiFR  
 H. Mattes  
 (coll. partner)  
Chalmers  
 P. Starski

CAY  
 A. Barcia  
 J.D. Gallego  
Ylinen, MilliLab  
 P. Kangaslahti  
 J. Tuovinen  
 M. Lahdes

### Project Goals :

**Develop cryogenic amplifiers with less than 5 x quantum limited noise up to 120 GHz, for low noise receiver applications. Advance technology development enabling future OSS and ESE missions up to 240 GHz**

- Optimize the structure and doping of InP HEMTs for cryogenic temperatures (~20 K) and higher frequencies
- Partner with other programs to reduce the cost of development ("pizza" masks) and frequent wafers to reduce cycle time; Work with TRW and URC foundries
- Produce many devices with less than 5 x quantum limited noise up to 120 GHz
- Fabricate amplifiers using hybrid MIC and MMIC technologies supporting multiple programs
- Evaluate the devices for gain stability and optimize

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## CHOP Status

The project has successfully produced discrete devices and MMICs with state-of-the-art performance:

Tens of thousands of discrete transistors supplying DSN and ground-based radio astronomy needs.

MMIC circuits from 1-200 GHz for a variety of applications including:

Planck, BEAST, ESE missions (AMLS), DSN and future DSN as well as non-NASA (FCRAO, foreign partners)

The program has completed 4 lots of wafers

2 lots of discrete wafers with record performance

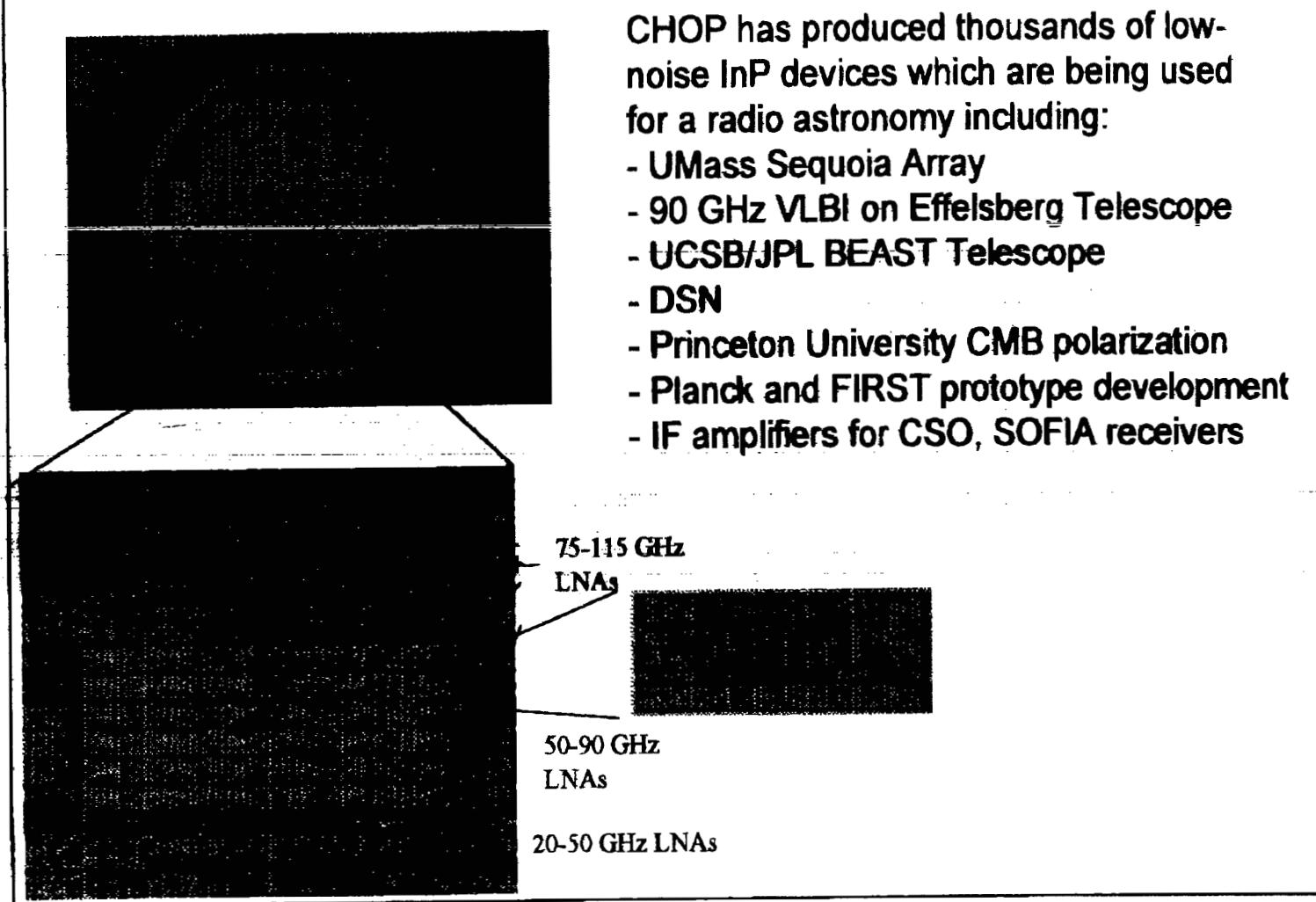
2 lots of MMIC wafers producing thousands of amplifiers with record performance

A new lot is in process. The program has been renewed by NASA for three years

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## Cryogenic HEMT Optimization Program





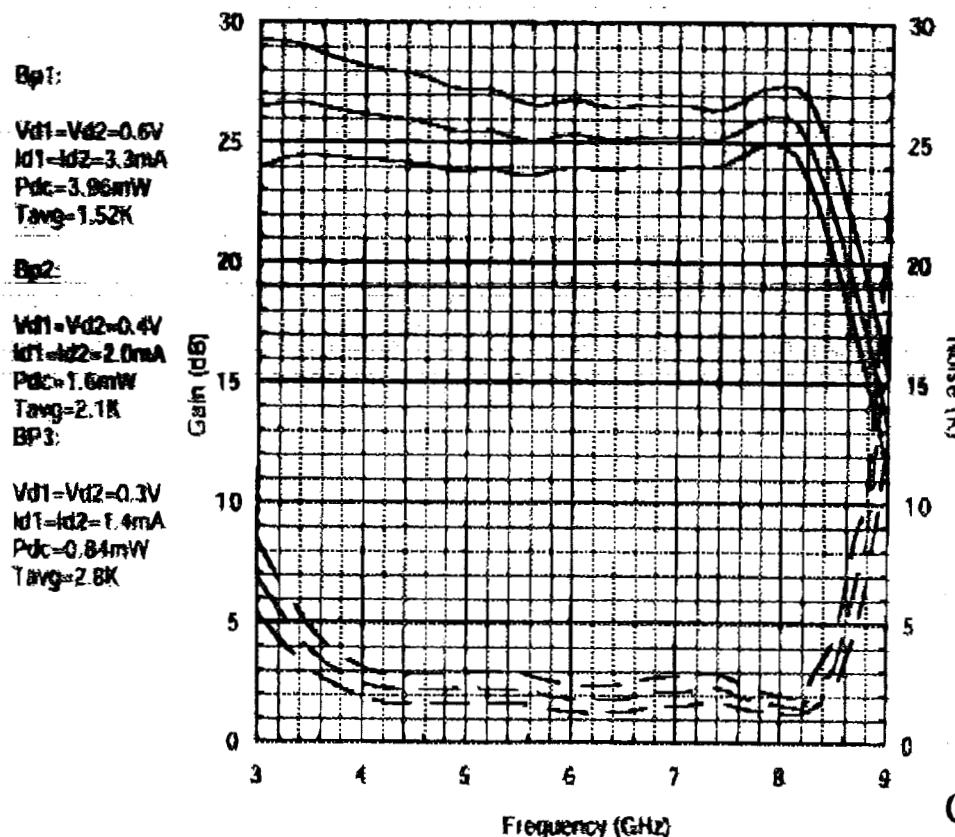
## Chalmers University 2-Stage LNA with TRW HEMTs

Gain (dB) bp1  
 Gain (dB) bp2  
 Gain (dB) bp3

Noise (K) bp1  
 Noise (K) bp2  
 Noise (K) bp3

Q1-Q2-TRW 0.1200  $\mu$ m hnp

4-8GHz LNA/JSC2 at 15K

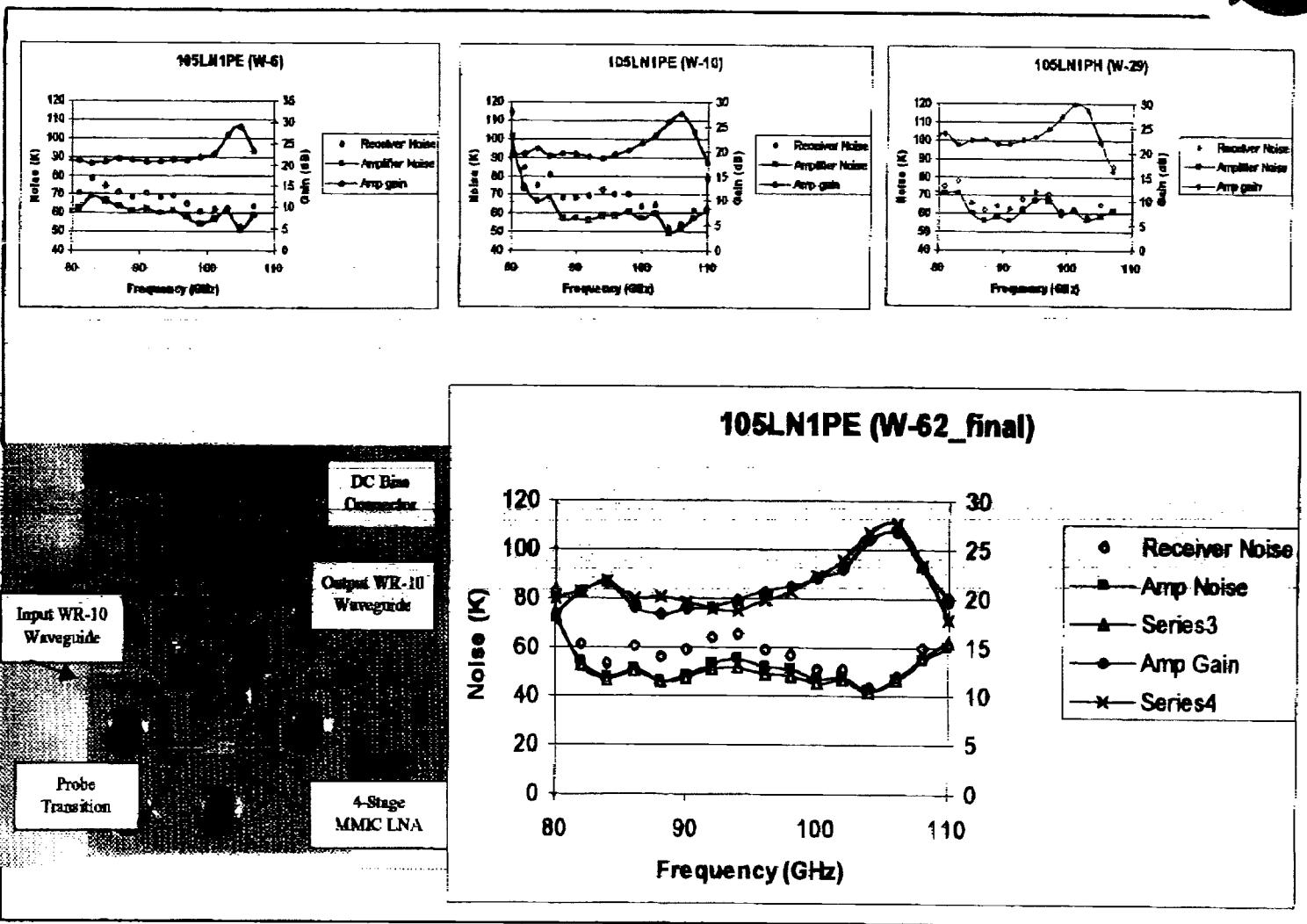


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Courtesy: P. Starski

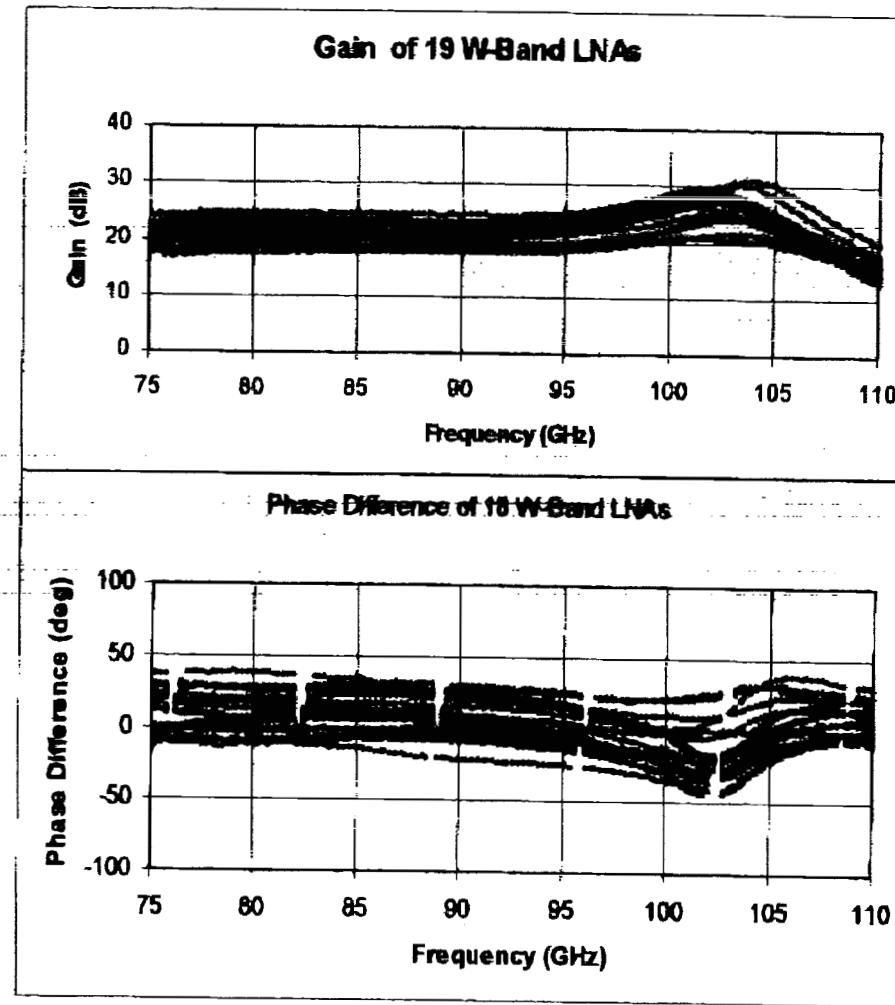


## Repeatable Amplifiers are Easily Built

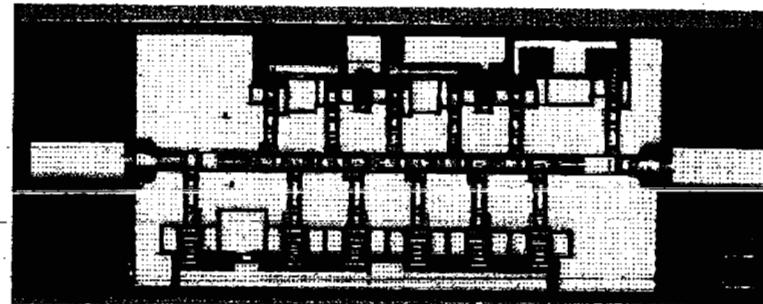
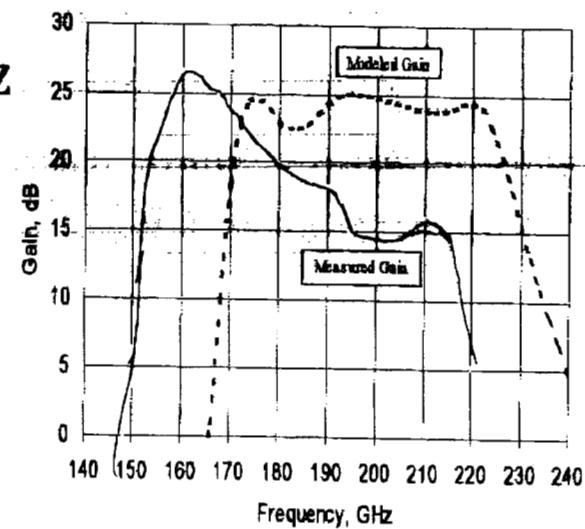




## MMIC Module Repeatability



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**JPL****200 GHz 6-Stage Low Noise Amplifier****Noise Figure 8 dB @170 GHz****0.03 mW  
250 GHz****NASA**

Ref: S. Weinreb et al IEEE-MGWL 7/99

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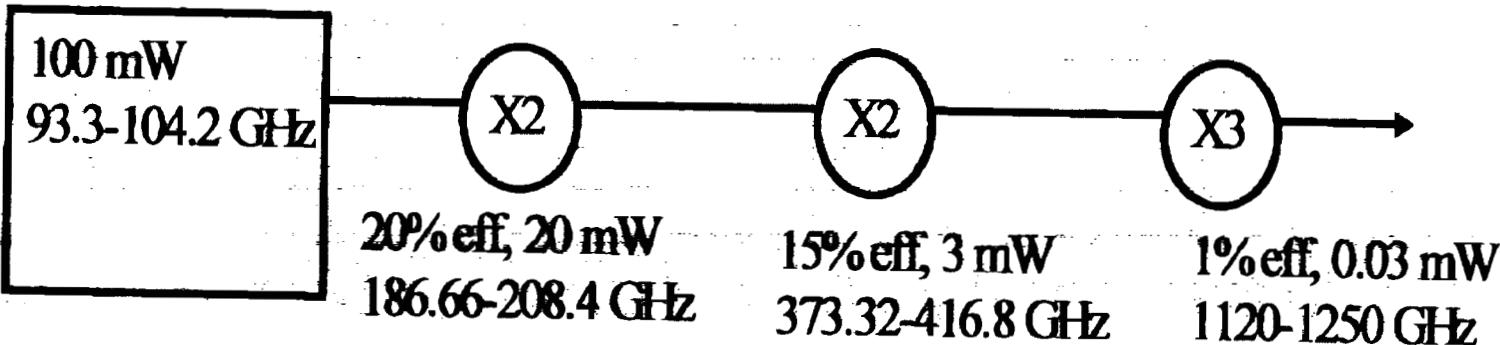


## Power Amplifiers



Power amplifier technology will play a key role in sub-mm heterodyne receivers, enabling broadband tunable local oscillators.

### *Baselined for FIRST and ALMA*



The current state-of-the-art allows power output of 500 mW at 100 GHz with efficiency of 15% or higher

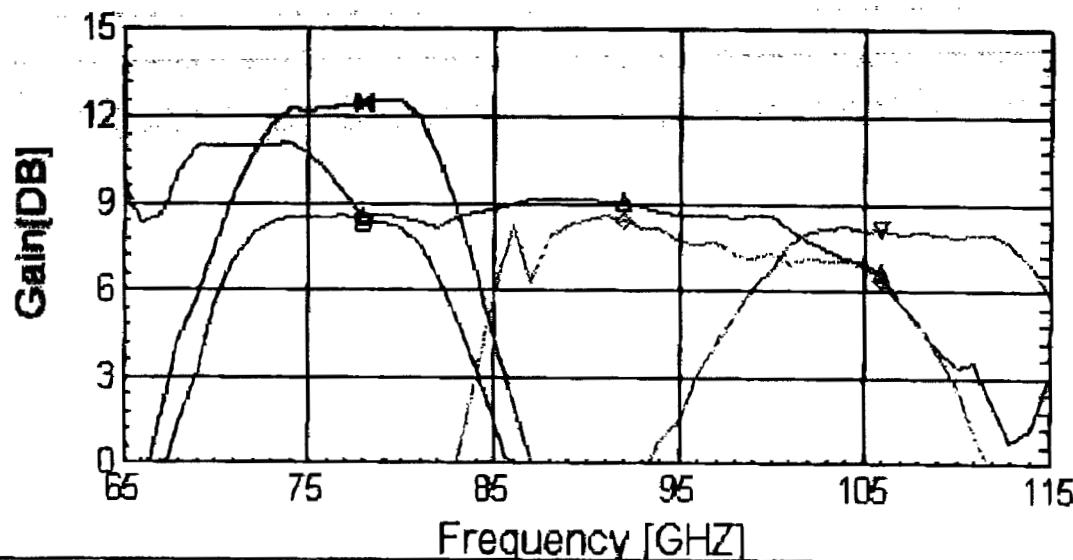
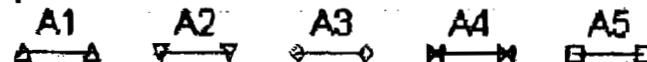
Technology includes GaAs and InP MMIC amplifiers with InP offering better efficiency



## FIRST Power Amps

- TRW GaAs foundry process
- 0.1 um PHEMT process
- 50 um thick substrate
- $f_t = 200$  GHz

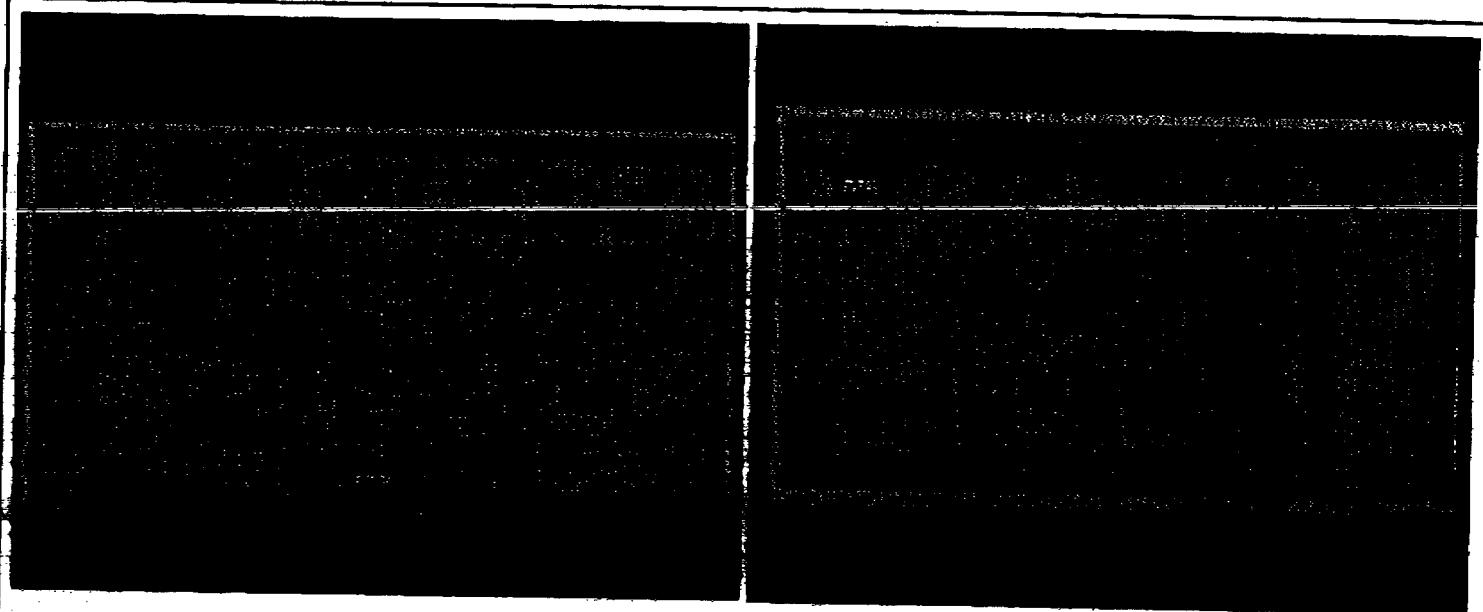
A combination of CPW medium power drivers, microstrip drivers, and high power drivers were used to achieve high output power



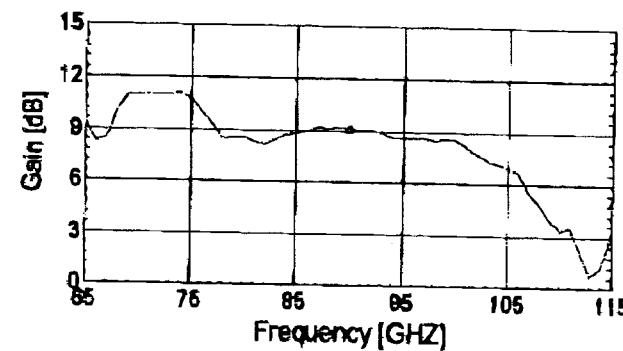
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## Driver Amplifiers



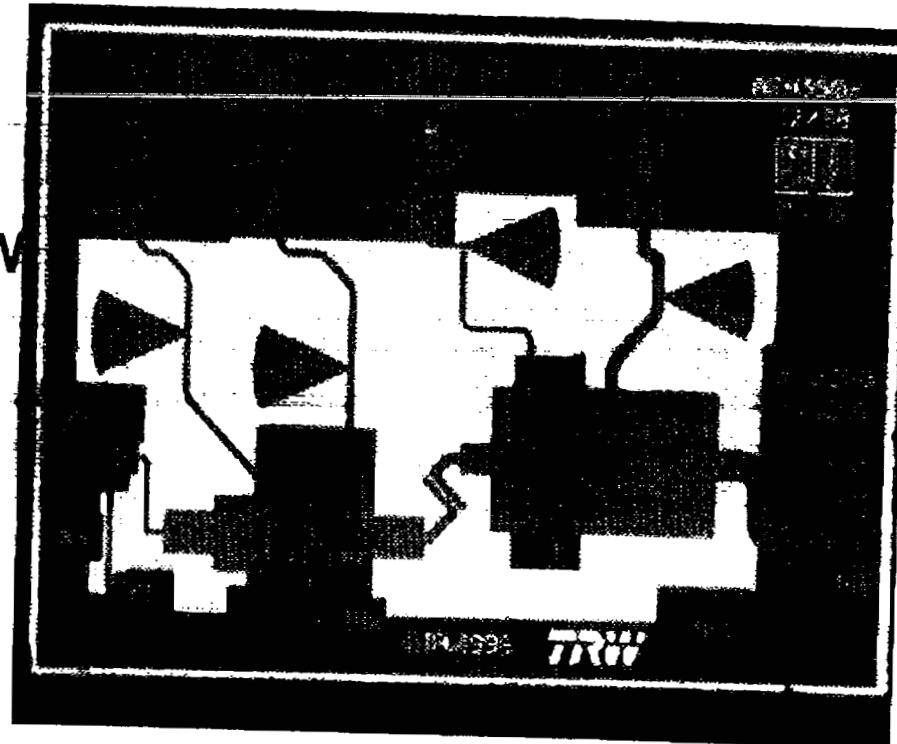
Pout = 25-50 mW  
Wide Band: 65-102, 80-115 GHz  
Gain: ~8 (+) dB



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**JPL****TRW High Power Driver Amplifiers**

- 32 finger device cell (output)
- Typical Pout ~ 100 mW
- 2.3 mm x 1.6 mm
- 10-15% Bandwidth



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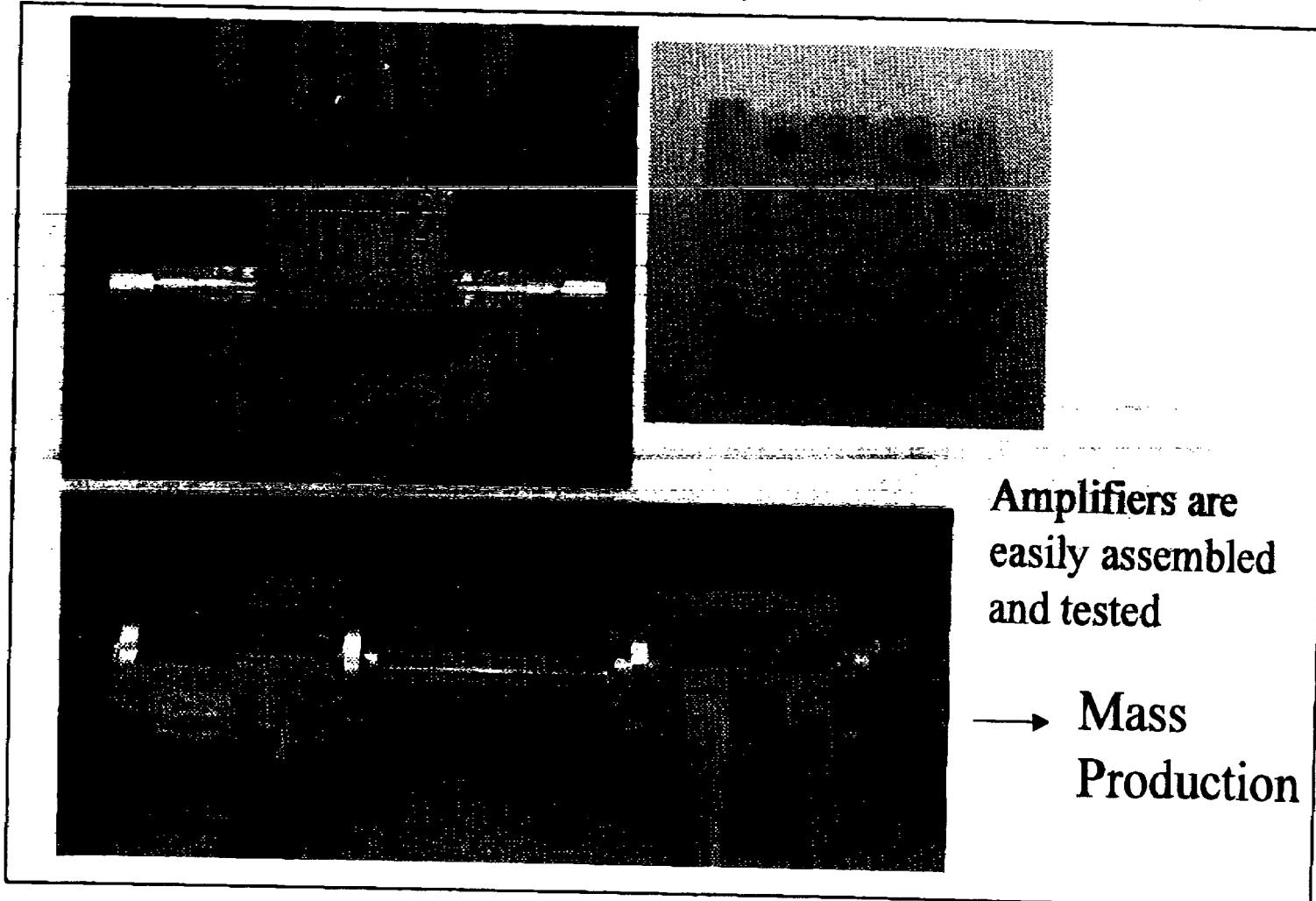
**JPL****TRW High Power Amplifiers**

- **64 finger device cell (output)**
- **1.28 mm periphery**
- **on-chip bias network**
- **50 ohm matching in/out**
- **2.3 mm x 1.6 mm**

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## Packaged Power Amplifiers



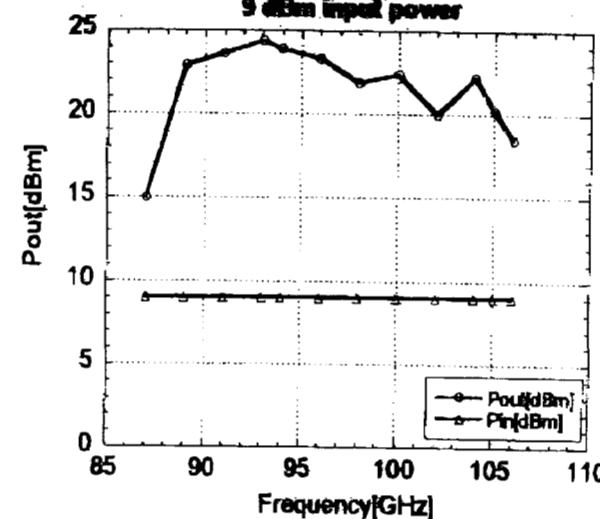
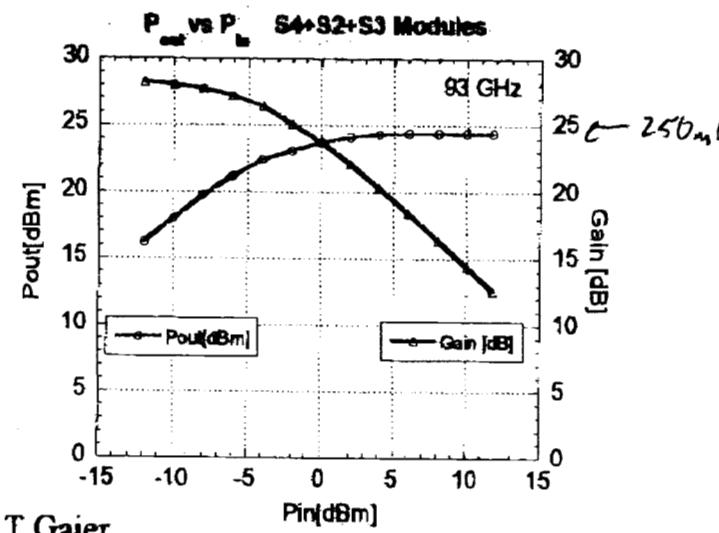
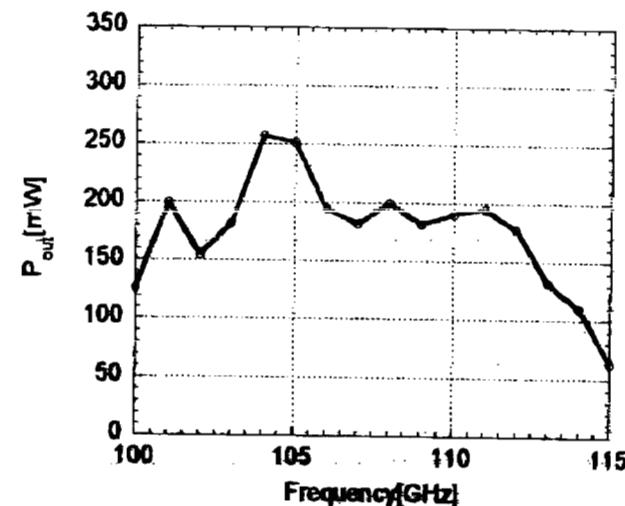
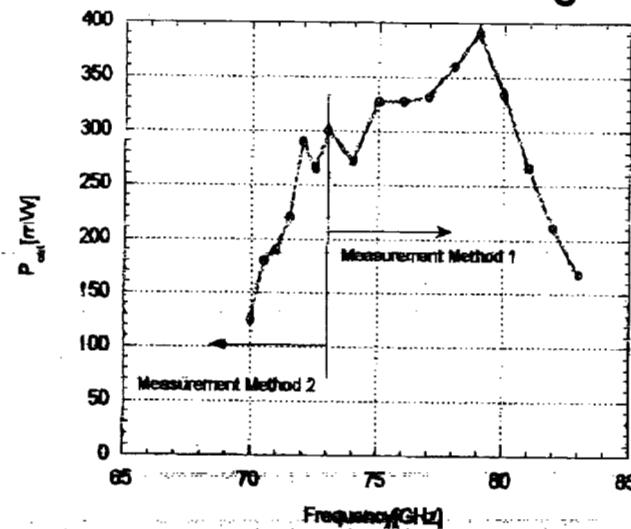
**Amplifiers are  
easily assembled  
and tested**

→ **Mass  
Production**

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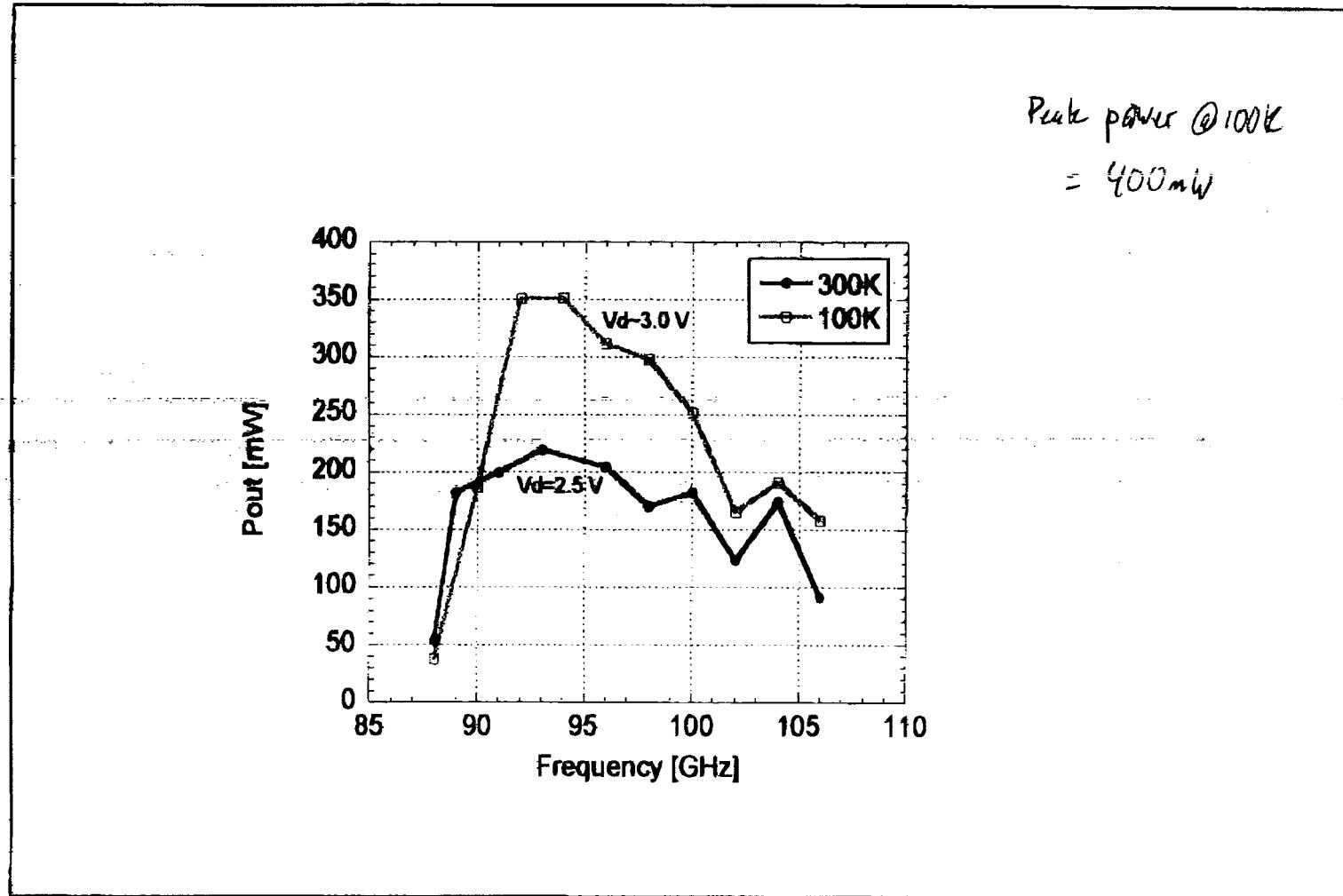
## Packaged Power Amplifiers



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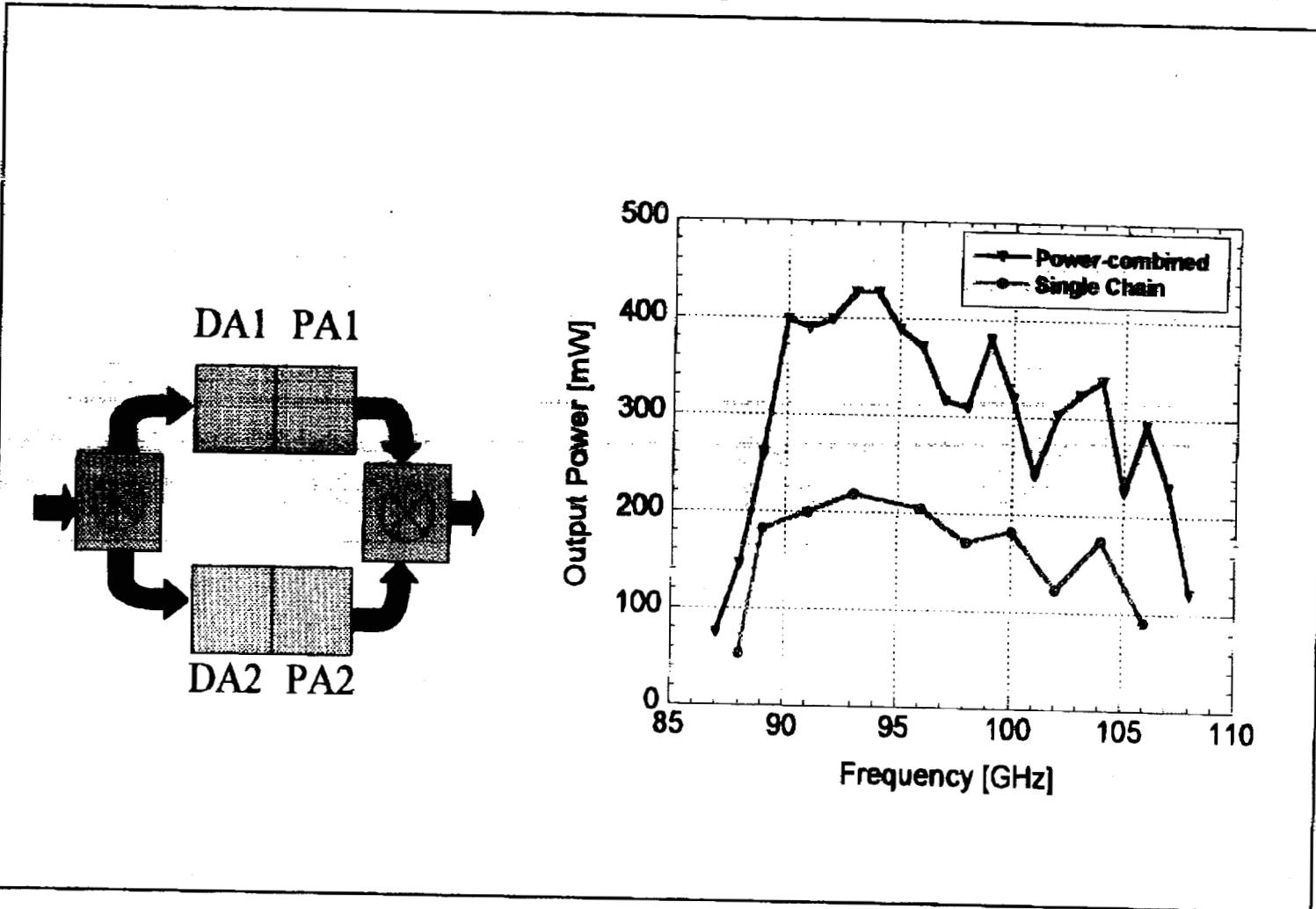
## Cryogenic Operation



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## Power Combining



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